REMARKS

Claims 1-16, all the claims pending in the application, stand rejected on prior art grounds. Applicants respectfully traverse these objections/rejections based on the following discussion.

I. The Prior Art Rejections

Claims 1-16 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Dobuzinsky et al. hereinafter "Dobuzinsky 246" (U.S. Patent No. 5,412,246) in view of Curran et al., hereinafter "Curran" (U.S. Patent No. 4,901,133). Claims 2-10 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Dobuzinsky 246 in view of Curan, and further in view of King et al., hereinafter "King"(U.S. Patent No. 6,479,862). Claims 11-16 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Dobuzinsky 246, Curran, King, and further in view of Dobuzinsky et al, hereinafter "Dobuzinsky 935" (U.S. Patent No. 5,330,935). Applicants respectfully traverse these rejections based on the following discussion.

A. The Rejection Based on Dobuzinsky 246 in view of Curran

Neither Dobuzinsky 246 nor Curran teach or suggest a structure that includes "a nucleation layer; a nitride layer on said nucleation layer; a re-oxide layer on said nitride layer" as defined by independent claim 1. Dobuzinsky 246 is fundamentally unrelated to the claimed invention and only discloses a low temperature plasma oxidation process and does not teach or suggest any aspect of the claimed structure. Curran also does not teach or suggest a two terminal device but instead merely shows a film for hermetically passivating monocrystalline silicon and is, again, fundamentally unrelated to the claimed invention.

Although the invention uses LPCVD process to fabricate SiN layer, the invention's stacked layer structure is still distinctly different from 5,412,246 (Dobuzinsky et al.). More specifically, Dobuzinsky 246 does not disclose the claimed "nucleation layer" or the separate

"nitride layer on said nucleation layer." Further, Dobuzinsky 246 is devoid of any form of re-oxide layer as defined by independent claim 1. The invention's stacked layer structure includes a first physical vapor deposition (PVD) thermal nitride nucleation layer on a heavily doped n+ substrate, followed by regular LPCVD SiN layer. The reason to use PVD before CVD is to improve SiN/Si interface and microstructure of the SiN layer. After LPCVD SiN deposition, a thermal oxidation of SiN was used to form a re-oxide layer instead of CVD deposition of Si02, which is different from 4,901,133 (Curran et al.). Furthermore, the multi-layer dielectric stack used in 4,901,133 was for hermetical passivation purpose. In contrast, the invention's dual layer SiN/re-oxide stack serves as an active device structure.

Therefore, the proposed combination of Dobuzinsky 246 and Curran does not teach or suggest "a nucleation layer; a nitride layer on said nucleation layer; a re-oxide layer on said nitride layer" as defined by independent claim 1. Therefore, Applicants respectfully submit that independent claim 1 is patentable over the proposed combination of references in the Office Action. In view the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

B. The Rejection Based on Dobuzinsky 246 in view of Curran and further in view of King

In rejecting independent claim 7 and dependent claims 2-6 and 8-10, the Office Action makes further reference to King for teaching a charge-trapping device. However, the invention's device structure, device electrical output characteristics, and the physics behind the device operation are fundamentally different from King's.

With respect to the claimed structure, King's device is a three-terminal MIS FET while the invention comprises a two-terminal MIM capacitor. The claimed two-terminal device offers advantages of easy integration, simple process, high density, and low-cost. The dielectric trapping layer in King's device was made on the top of a p+ substrate. Thus, King's charge traps were located relatively close to Si-dielectric interface with non-uniform trap density across the

dielectric (traps were centered at the location close to Si-dielectric interface) so that hot charges from Si channel could be trapped and dc-trapped very quickly. However, the invention's dielectric trapping layer is made on the top of n+ substrate that is covered with a nucleation layer. This allows the invention's traps to be placed far away from the Si-dielectric interface and to be uniformly distributed across the dielectric since the invention's space-charge limited conduction does not require quick trapping and dc-trapping mechanism.

With respect to the physics of device operation, although King's device also used "trap" concept, its physics of device operation is different from the invention's. Since King's device is a 3-terminal FET, in order to generate NDR characteristic, it relies on the quick "trapping" and "dc-trapping" mechanism to capture and release "hot carriers " (energetic carriers) created by high composite electric field (channel + gate field) in the channel. This mechanism is further modulated by gate field. To the contrary, with the claimed structure, the invention's carriers are "cool" instead of "hot" due to direct tunneling instead of "hot carrier" injection. Single gate field controls the "cool" electron injection (no channel field is required). The invention's "trapping" mechanism dominates during the device operation and "de-trapping" is insignificant during the device operation. Therefore, with the claimed invention, the location of those traps could be anywhere in the dielectric system. After the invention's traps are all filled, a sudden current jump occurs with almost no voltage change.

King's device generates conventional NDR characteristics (see King's Figure 2) while the invention's device generates a unique sudden current jump at a constant voltage during operation (see Applicants' Figures 2 and 4). Such constant voltage output under large current swing is ideal for voltage regulator application. In addition, due to the invention's capacitor configuration nature, it also could serve as a decoupling capacitor to minimize ripple of the AC current, which is another important function in power supply circuit.

Therefore, by using just one single device in a power supply circuit, the invention can achieve two important functions. In addition to power supply application, the invention also could be used a process monitor to better control the semiconductor gate dielectric fabrication process. On the other hand, King's device is good for high density memory and logic

application, as well as power management (low power application but not for power supply application, which have two different concepts).

Therefore, Applicants respectfully submit that the proposed combination of references does not teach or suggest "a nucleation layer; a nitride layer on said nucleation layer; a re-oxide layer on said nitride layer" as defined by independent claims 1 and 7. Therefore, independent claims 1 and 7 are patentable over the prior of record. Further, dependent claims 2-6, and 8-10 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

C. The Rejection Based on Dobuzinsky 246 in view of Curran, King, and further in view of Dobuzinsky 935

The two Dobuzinsky references are fundamentally unrelated to the claimed structure and methodology, and the Office Action provides little explanation as to how either of these references may apply to the claimed invention. More specifically, Dobuzinsky 246 and Dobuzinsky 935 disclose low temperature plasma oxidation processes and do not teach or suggest the claimed methodology that includes "thermally growing a nucleation layer on a substrate; performing a low pressure chemical vapor deposition (LPCVD) of silicon nitride on said nucleation layer; and re-oxidizing a top portion of said silicon nitride to form a re-oxide layer" as defined by independent claim 11. Further, as also shown in detail above, neither Curran nor King teach or suggest a structure process that uses the claimed thermally grown nucleation layer as the claimed invention does.

Therefore, it is Applicants' position that the applied prior art of record does not teach or suggest "thermally growing a nucleation layer on a substrate; performing a low pressure chemical vapor deposition (LPCVD) of silicon nitride on said nucleation layer; and re-oxidizing a top portion of said silicon nitride to form a re-oxide layer" as defined by independent claim 11.

Thus, Applicants respectfully submit that independent claim 11 is patentable over the prior of record. Further, dependent claims 12-16 are similarly patentable. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

II. Formal Matters and Conclusion

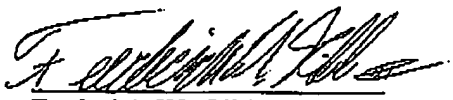
In view of the foregoing, Applicants submit that claims 1-16, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

Dated: 2/24/04



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